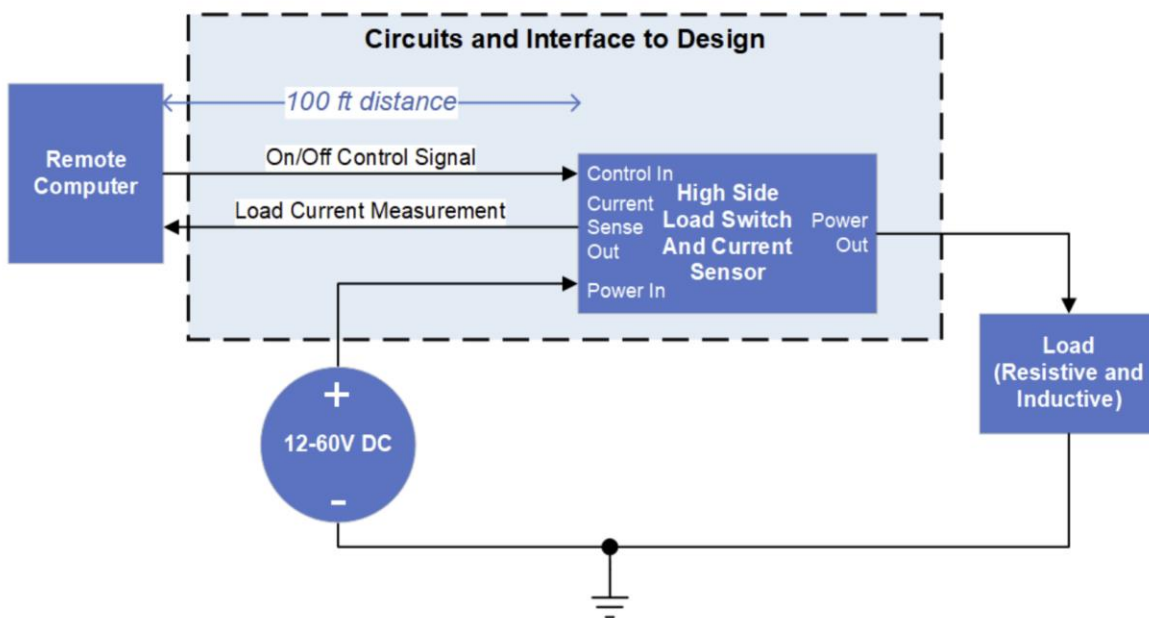# Remote Load Switch

Design Notes

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jkailimcnelly@gmail.com

Design Requirements

This design is required to switch 12-60VDC power into a resistive and inductive load ($L_{load} \leq 5mH$). Control signals must be received from, and load measurements with a resolution of 10mA must be reported to, a remote control computer up to 100ft away. The switch must be capable of operating continuously and may be cycled on and off at a frequency lower than 1Hz. The overall design should be tolerant of temperatures between -40°C to +70°C, standard atmospheric pressure, some conducted and radiated EMI, and moderate mechanical shock and vibration.


More detailed requirements for the load switch, current sensing, and remote interface are provided on the following page

Design Approach
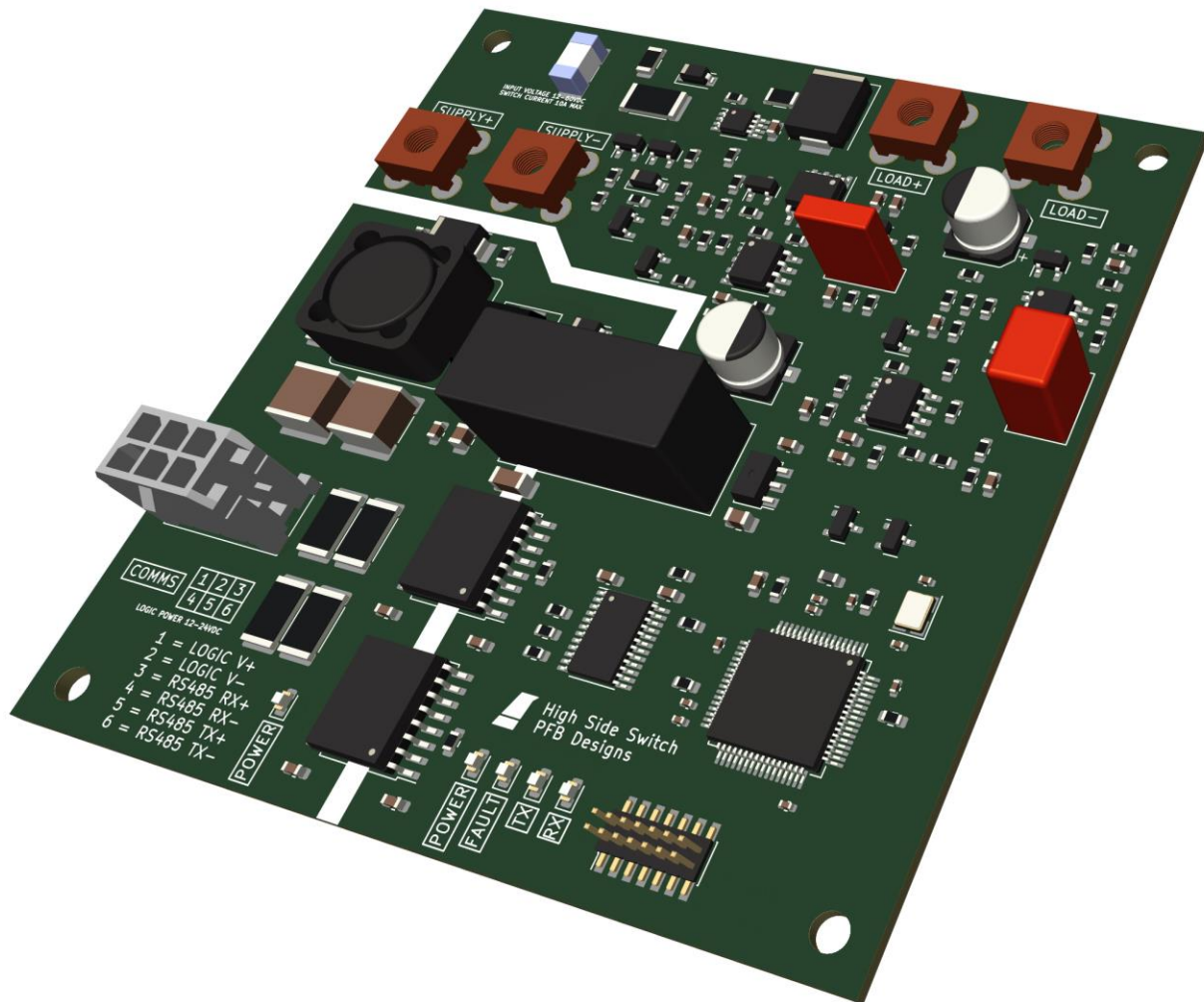
The High Side Switch device was designed to meet the performance criteria with simplicity and reliability in mind. Critical components such as switching transistors and power dissipating elements are oversized for the nominal use case and adequately derated for their operating environment. A number of operating scenarios that could result in potentially severe electrical failure modes were anticipated during the design process, and mitigated through the addition of circuitry that protects the device from undervoltage of the load power supply and two distinct load overcurrent scenarios (fast / slow overcurrent protection). In scenarios where protection of the device from damage was not possible within the design constraints, such as severe overvoltage (>100V), failure modes were deliberately engineered to encourage the device to fail into a "safe" state (i.e. load disconnected from the power supply).

The High Side Switch's protection and sensing circuitry relies entirely on analog circuits in order to trigger device protections and filter measured values. This results in a simple, fast-acting, continuously-monitoring system that performs internal protection functions regardless of the state of the onboard microcontroller. This also means that the required firmware for this device is simple and has very low performance requirements, as it only needs to handle device communication and monitor a latching fault bus a few times per second.
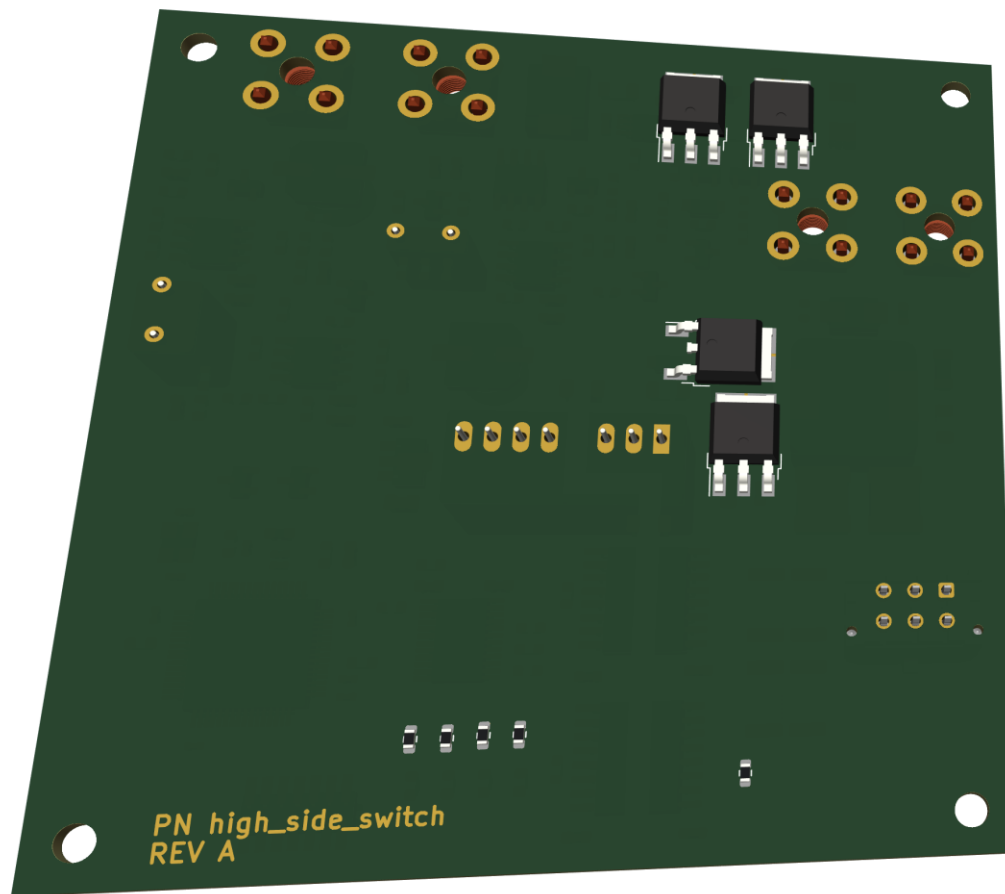
The High Side Switch is intended to be mounted into a metal enclosure for environmental protection. Heat-dissipating components are installed on the bottom of the board in order to allow easy cooling to an enclosure chassis with thermal pads or similar materials. Data connections are made with automotive-grade wire to board connections (intended for connection to a panel-mounted aerospace-grade enclosure connector). Power connection points are designed with high current board-mounted screw terminals in order to provide direct connections to ring terminals and associated enclosure-mounted aerospace-grade connectors.

System-level protection and ease of use were also considered during design of the High Side Switch. By isolating communications power and data from the load power supply, the High Side Switch can be utilized in systems where the load and the remote control computer have different common mode voltage potentials. Additionally, galvanic isolation between these nets ensures that the High Side switch will not serve as a common ground point between the two systems, thereby removing the potential for ground loops. Operation of the High Side Switch with a shared power supply is also possible, with no extra steps required for installation or use.

The High Side Switch utilizes an isolated UART over RS-485 interface for communication, in order to simplify requirements for the remote control computer to a single interface that is used for switch control, current measurements, and error monitoring. The High Side Switch is intended to be used in a single-master RS-485 connection, with a point to point connection between the High Side Switch and the remote computer, and no other devices on the bus (remote computer is the master).

The High Side Switch favors discrete design with readily substitutable general-purpose components in order to manage costs and provide a robust supply chain for long-term producibility.

Design Explanation
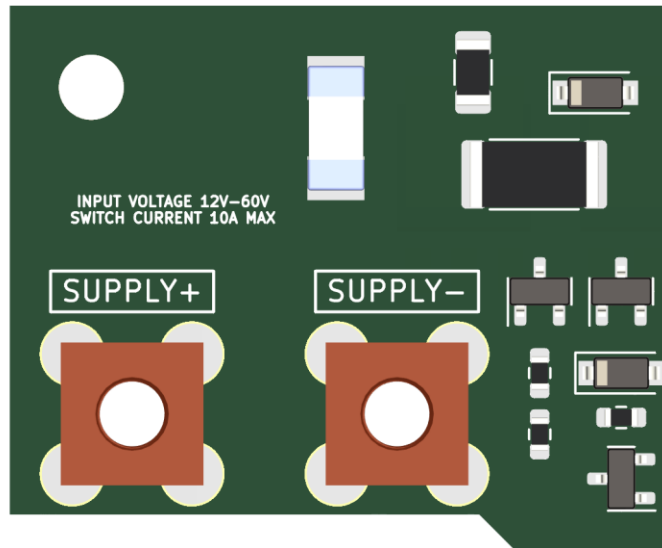
System Power Input

Schematic
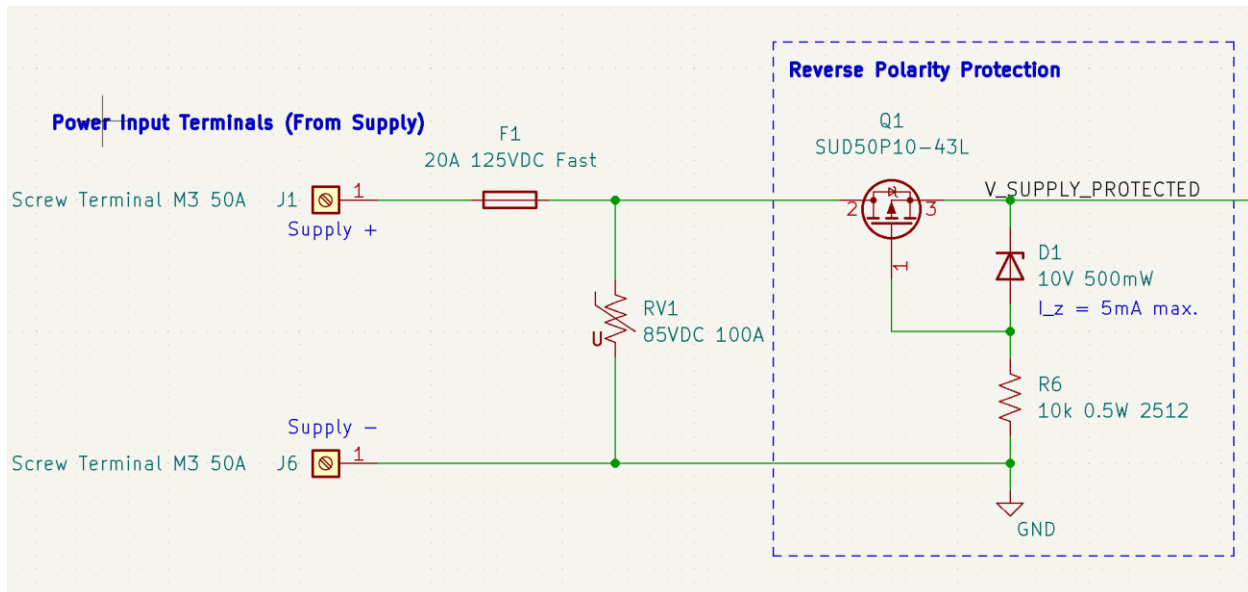
System power is protected against reverse polarity using a PMOS transistor connected drain-first. In the nominal polarity configuration, current flows through the PMOS body diode and then through the Zener diode (D1) and current limiting resistor (R6), generating a -10V gate-source voltage on the PMOS transistor that turns on the MOSFET. In the reverse polarity configuration, current flows up through the current limiting resistor and the diode, generating a +Vf gate-source voltage on the PMOS transistor that turns it off, where Vf is the forward voltage of the Zener diode (D1).

Auxiliary protection against overvoltage and overcurrent is provided with a 20A fuse (F1) and a metal oxide varistor (RV1). The varistor is designed to crowbar the supply rails and blow the fuse during an overvoltage event, thereby disabling the circuit's power input and reducing the likelihood that an overvoltage event causes the primary PMOS switch to fail closed. The fuse also provides protection in the case that downstream overcurrent protection circuitry fails to open the main PMOS transistor during an overcurrent event. The fuse current rating and trip curve is selected such that it takes significantly longer to trip than the overcurrent protection circuitry during a large current spike, thereby reducing the chance of false positive fuse blown events.

Calculations

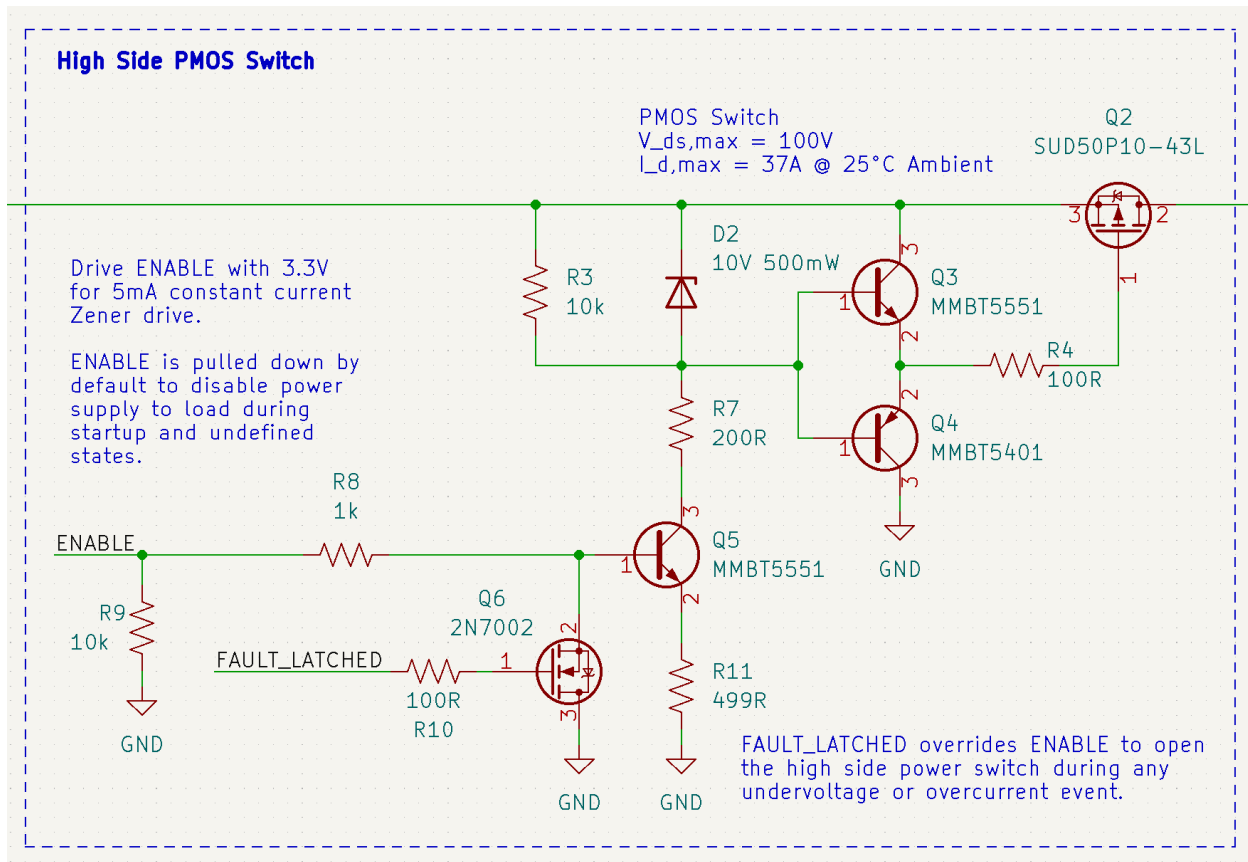| Reverse Polarity Protection			
V_rp,gs	10	V	Gate source voltage of PMOS in reverse polarity protection circuit.
I_rp,zener	5	mA	Current through reverse polarity protection zener diode with max supply voltage in nominal polarity.
R_rp	10	kOhms	
P_rp,resistor	0.25	W	Power dissipated in reverse polarity protection gate drive resistor.
P_rp,zener	0.05	W	

PCB Layout

System power (i.e. the power connected to the load) is fed into the remote load switch via high-current M3 screw terminals bonded directly to the PCB.

Load Switch

Schematic

High Side PMOS Switch

PMOS Switch
V_ds,max = 100V
I_d,max = 37A @ 25°C Ambient

Q2
SUD50P10−43L

D2
10V 500mW

R3
10k

Q3
MMBT5551

R4
100R

Drive ENABLE with 3.3V
for 5mA constant current
Zener drive.

ENABLE is pulled down by
default to disable power
supply to load during
startup and undefined
states.

R7
200R

Q4
MMBT5401

R8
1k

ENABLE

Q5
MMBT5551

GND

R9
10k

Q6
2N7002

FAULT_LATCHED

R11
499R

R10
100R

GND

GND

GND

GND

FAULT_LATCHED overrides ENABLE to open
the high side power switch during any
undervoltage or overcurrent event.

The load switch uses a PMOS transistor to control the current flowing to the load through the positive supply rail. Gate drive of the PMOS transistor is achieved with a Zener diode (D2) and pullup resistor (R3) which synthesize a -10V gate voltage and a totem pole BJT pair (Q3 and Q4) used for fast gate drive. A gate resistor (R4) can be used to adjust gate resistance to limit EMI and damp oscillations in the PMOS transistor.

Normally, the Zener diode (D2) in this circuit would be pulled to ground through a single current limiting resistor, but the wide power supply voltage range would result in widely variable Zener currents (and hence, variable power dissipation in the current limiting resistor). This would make turn-on time and gate voltage dependent on supply voltage, and would make the power dissipated in the current limiting resistor proportional to the square of the supply voltage ($P = V^2/R$). A BJT current source (Q5) is used in conjunction with a constant base drive voltage (3.3V) to hold the Zener current steady while supply voltage varies. This makes the power dissipated in the current limiting resistor and the BJT dependent on supply voltage, but only linearly as current remains constant ($P = IV$). Care is taken to select a Zener drive current such that the Zener turns on quickly and is fully saturated, while not exceeding power dissipation requirements in Q5 during high voltage supply scenarios. The simulation plot below shows current through the Zener diode (plotted in red) holding steady while supply voltage varies (plotted in green).

The PMOS transistor is turned on and off by toggling the ENABLE line connected to the base of Q6. ENABLE has a base resistor to limit current into Q6, as well as a pulldown resistor to make sure the PMOS transistor is OFF during startup and undefined states.

System faults can override the PMOS transistor with a fail-open behavior by pulling ENABLE to ground via Q6 whenever the FAULT_LATCHED line is HI.
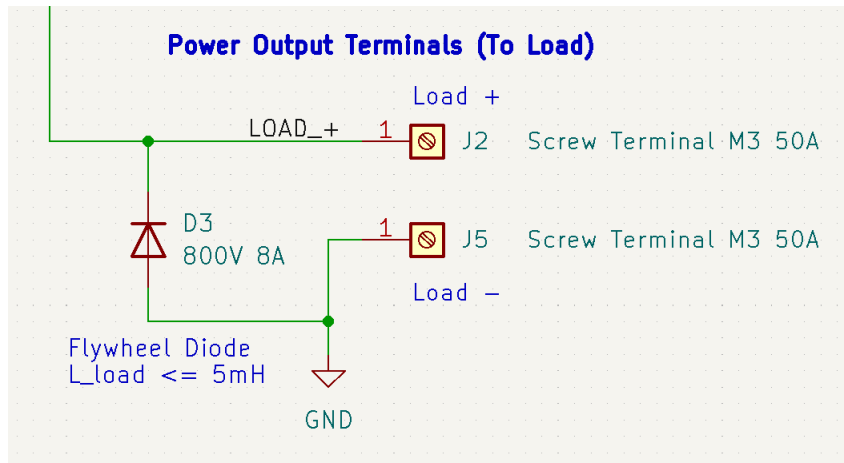

A flywheel diode is included across the power output terminals in order to protect the PMOS switch and other components from voltage spikes caused by switching an inductive load.

Calculations

| PMOS Switch Parameters			
V_logic,high	3.3	V	
P_switch,max	5.8	W	Max power dissipation allowed in PMOS switch at max rated temperature.
PMOS Gate Drive			
V_drive,zener	10		
P_drive,zener	0.05	W	Power rating for gate drive zener.
I_drive,zener	5	mA	
V_drive,be	0.8	V	
R_drive,e	500	Ohms	Emitter resistor to set zener current for gate drive.
R_drive,c	200	Ohms	BJT collector resistor.
P_drive,c	0.005	W	Power absorbed by dissippation resistor on BJT collector.
V_drive,ce,max	46.5	V	Collector-emitter voltage across current source BJT.
P_drive,bjt	0.2325	W	Power dissipated in gate drive BJT while turned ON with max supply voltage.
V_drive,headroom,min	4.3	V	Minimum voltage used by drive circuitry (e.g. during low supply voltage operation). MOSFET gate drive voltage will be limited to V_supply,max - V_drive,headroom,min.
Low Supply Voltage Gate Drive Scenario			
R_switch,ds,on,lv	0.048	Ohms	R_ds,on of PMOS switch in low supply voltage scenario. Gate drive zener is not fully saturated so this corresponds to the max R_ds,on of the PMOS switch.
P_switch,lv	4.8	W	Power dissipation in PMOS switch with max load current in low supply voltage scenario.

PCB Layout
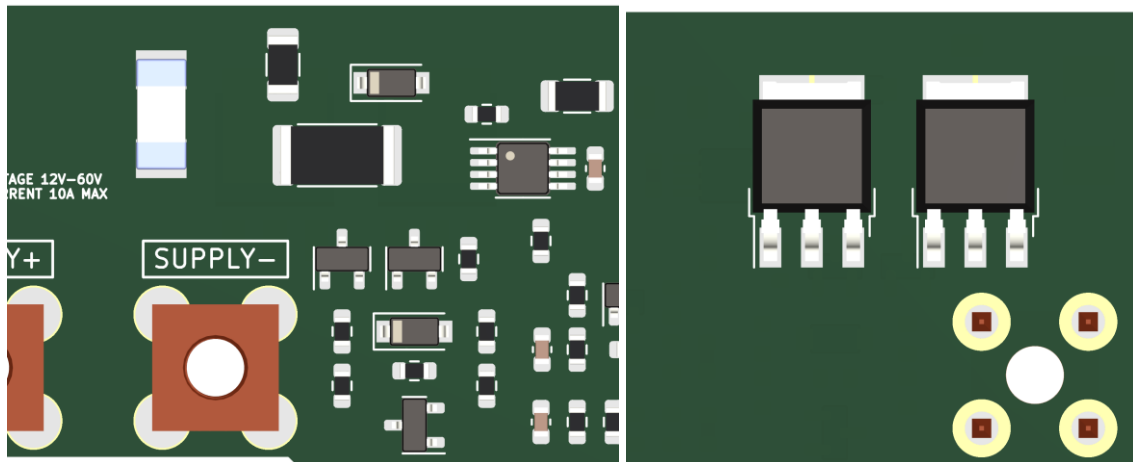
The load switch drive components are located on the top of the PCB adjacent to the system power supply input. Both the reverse polarity protection PMOS and the load switch PMOS are located on the bottom side of the board to allow heatsinking to a metal enclosure.

Current Sense

Schematic
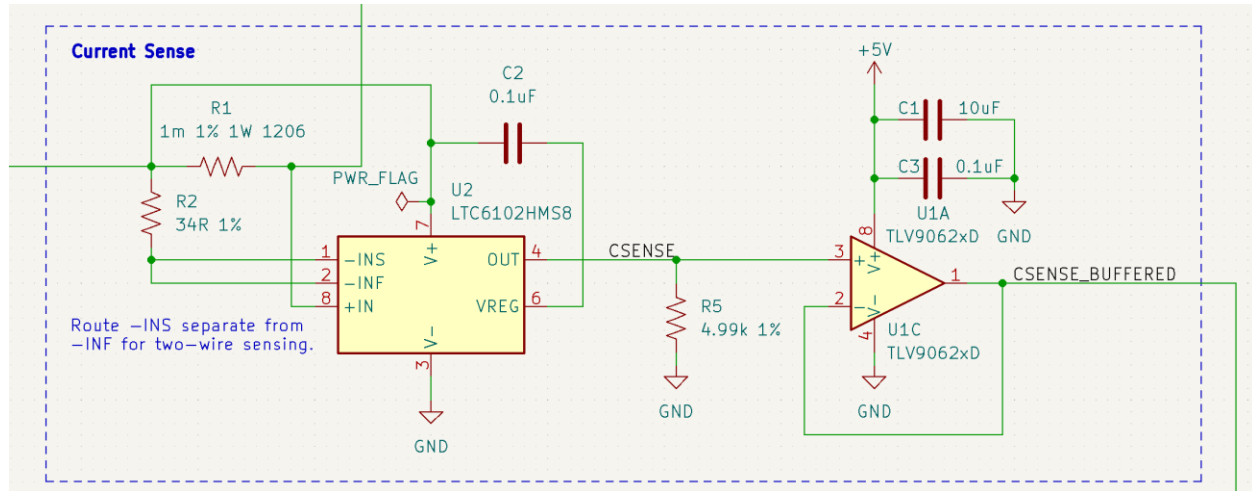
Current sensing is achieved with an LTC6102 high-side zero-drive precision current sense amplifier. This IC has an internal op-amp control circuit that matches the voltage drop across the sense resistor (R1) with the voltage drop across and input resistor (R2). The current flowing through the input resistor is then fed into an output resistor (R5) which creates a GND-referenced analog voltage that is proportional to the current flowing through the sense resistor.

The current sense voltage CSENSE is buffered by a TLV9062 rail-to-rail op amp to prepare it for further distribution and filtering elsewhere in the circuit.

Calculations

Current Sense Amplifier Parameters			
R_csense	1	mOhms	Current sense shunt resistor value.
V_csense,max	0.01	V	Must be below max LTC6102 input voltage.
V_csense,min	10	uV	Must be above LTC6102 input offset voltage (~3uV).
R_in	34	Ohms	LTC6102 input resistor value.
I_rin,max	0.294	mA	
R_out	4.99	kOhms	LTC6102 output resistor value.
V_out	1.47	V	Current sense voltage during nominal max current load.
N_bits,adc	12	bits	
V_max,adc	3.3	V	
I_resolution,adc	5.5	mA	
A_csense	0.147	V/A	Current sense voltage to load current gain: V_out / I_load.

Note that in the maximum load current scenario, the output of the current sense amplifier is only 1.47V, since additional headroom is needed in order to measure current for triggering overcurrent protection at 150% and 300% nominal load current thresholds. Even with this reduced output voltage range, a 12-bit ADC can theoretically get 5.5mA resolution (but it probably won't be pretty). If high resolution current sense is a strong driving requirement, additional amplification (with a 3.3V rail) could be added with another op-amp stage before the microcontroller ADC input.

Overcurrent Detection

Schematic
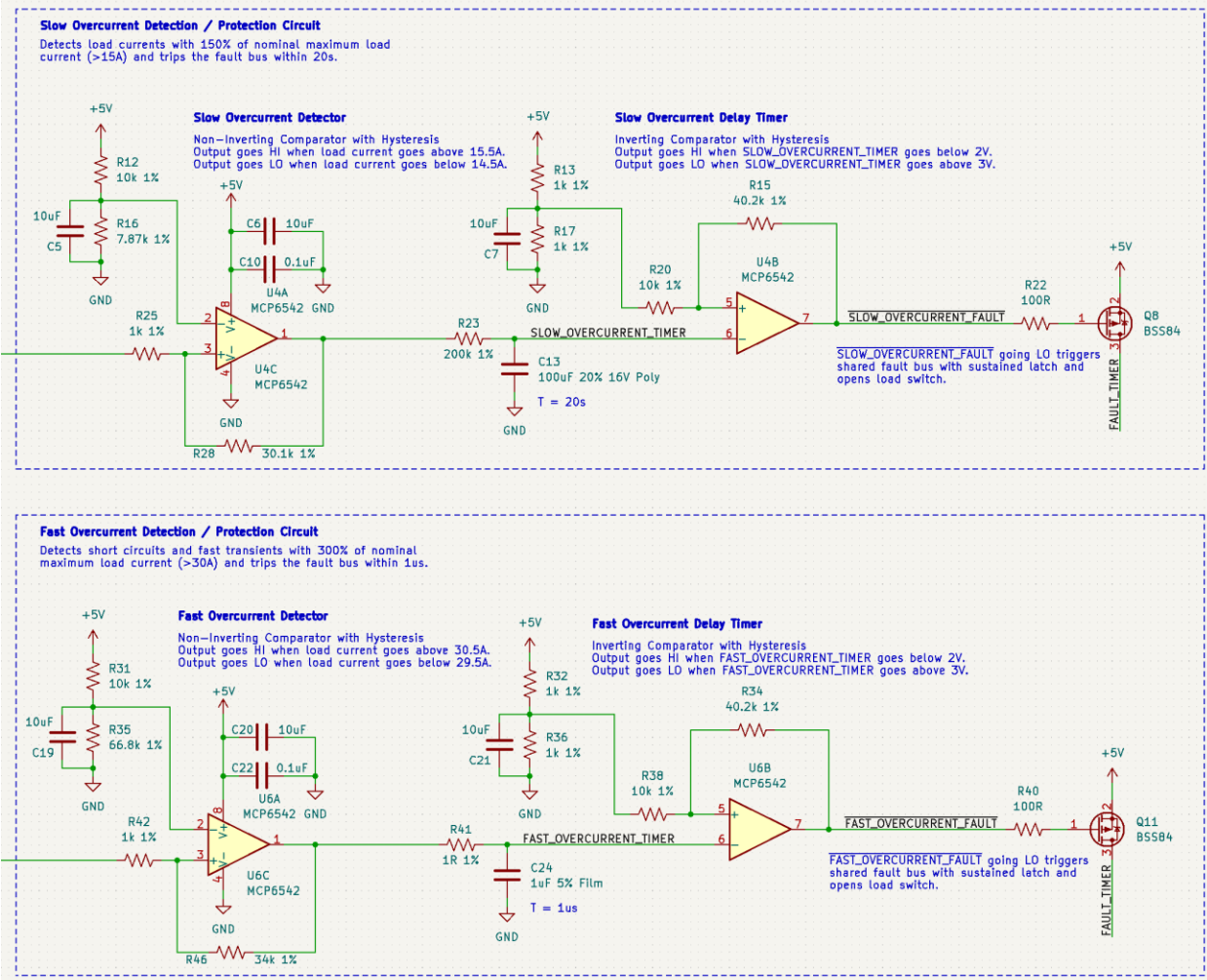
Overcurrent protection is provided with two separate thresholds and trip times, a 300% (30A) for 1us trip threshold (fast overcurrent protection), and a 150% (15A) for 20s trip threshold (slow overcurrent protection). This approximately mimics the trip curve of a B-curve circuit breaker, and allows for protection of the PMOS switch wiring harnesses running to the supply or load, and downstream / upstream devices. Fast overcurrent protection is intended to guard against short circuits (fast time constant) while keeping the trip current high enough that it does not get tripped by the inrush current of typical capacitive loads (similar function to the coil of a circuit breaker). Slow overcurrent protection is intended to guard against continuous overcurrent that could result in thermal damage (slow time constant, low trip current threshold, similar to the thermal trip mechanism inside a circuit breaker).

The slow overcurrent protection circuit first feeds the current sense signal into a current comparator (U4A), which determines whether the slow overcurrent threshold is currently being exceeded. If it is, the current comparator charges an RC timing circuit with a specifically designed rise time. Once this timing circuit charges to a voltage that exceeds the trip threshold of the connected timer comparator (U4B), a slow overcurrent fault is asserted on the SLOW_OVERCURRENT_FAULT bus, which turns on a PMOS signal MOSFET to charge up the shared FAULT_TIMER bus. This FAULT_TIMER bus results in the fault being latched for a set period of time, which reports the issue to the microcontroller, illuminates a FAULT indicator LED, and disables the load PMOS switch.

The fast overcurrent protection circuit works identically to the slow overcurrent protection circuit, except that the timing circuit has different values (for a faster time constant), and the trip threshold on the current comparator is higher (300% overload current, instead of 150%).

All comparators used in these circuits (and the rest of the design) include hysteresis in order to avoid oscillation when crossing a trip threshold. Comparator reference voltages are synthesized with a resistive divider and a filter cap to reduce fluctuations due to noise. Dual comparators are used in order to reduce layout space claim and improve PCB routing.

Calculations

Overcurrent Protection Parameters			
V_oc,top	5	V	Reference voltage at top of resistive divider for overcurrent threshold.
I_oc,hysteresis	0.50	A	Hysteresis band (one side) for overcurrent protection.
V_oc,hysteresis	0.07	V	Hysteresis band (one side) for overcurrent protection.
V_oc,oh	5	V	Overcurrent comparators output high voltage.
R_oc,ref,top	10	kOhms	
Fast Overcurrent Protection Comparator			
t_rise,oc,fast	1.00E-06	s	Trip time for fast overcurrent protection (3x overcurrent). 0.63*V_s = 1T
C_oc,fast	1	uF	Slow overcurrent protection timing cap.
R_oc,fast	1	Ohms	
CR_oc,fast	300	%	Current Ratio for fast trip threshold.
I_oc,fast	30	A	Fast overcurrent trip threshold.
V_oc,fast	4.40	V	Trigger voltage for fast overcurrent protection.
R_oc,fast,in	1	kOhms	Input resistor value for fast overcurrent protection comparator.
V_oc,fast,tlh	4.48	V	Low high transition voltage for fast overcurrent protection.
V_oc,fast,thl	4.33	V	High low transition voltage for fast overcurrent protection.
V_oc,fast,ref	4.35	V	
R_oc,fast,f	34	kOhms	Feedback resistor value for fast overcurrent protection comparator.
R_oc,ref,bot,fast	66.8	kOhms	Cap in parallel with bottom resistor in voltage sense divider for low pass filter.
Slow Overcurrent Protection Comparator			
t_rise,oc,slow	20	s	Trip time for slow overcurrent protection (1.5x overcurrent).
C_oc,slow	100	uF	
R_oc,slow	200	kOhms	
CR_oc,slow	150	%	Current Ratio for slow trip ratio.
I_oc,slow	15	A	Slow overcurrent trip threshold.
V_oc,slow	2.20	V	Trigger voltage for slow overcurrent protection.
R_oc,slow,in	1	kOhms	Input resistor value for fast overcurrent protection comparator.
V_oc,slow,tlh	2.27	V	Low high transition voltage for fast overcurrent protection.
V_oc,slow,thl	2.13	V	High low transition voltage for fast overcurrent protection.
V_oc,slow,ref	2.20	V	
R_oc,slow,f	30	kOhms	Feedback resistor value for fast overcurrent protection comparator.
R_oc,ref,bot,slow	7.9	kOhms	Corner frequency of voltage sense low pass filter.
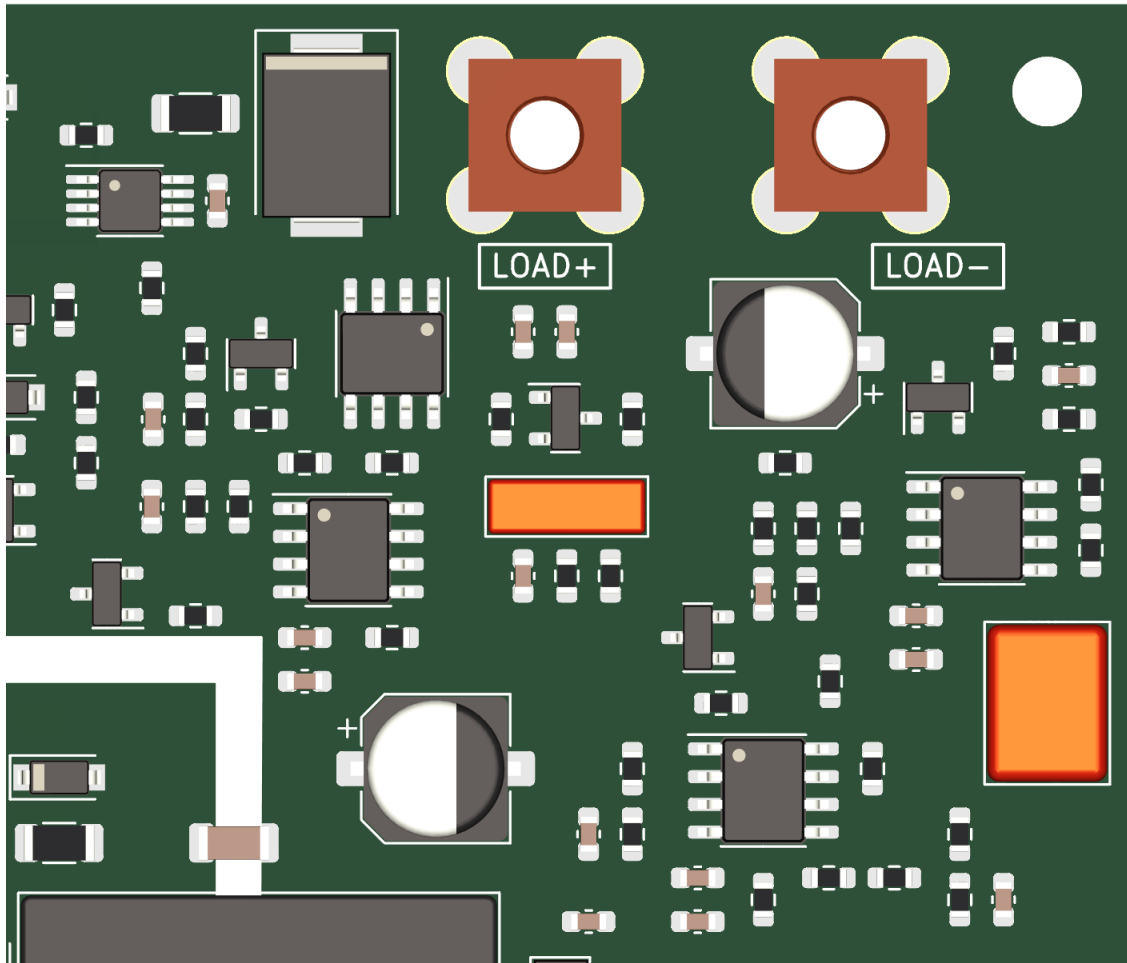
Nothing that special. Timing caps are Mylar for better accuracy / no voltage dependent weirdness. Large 100uF timing cap is polymer, since a Mylar cap of that size would be very expensive and a looser timing spec for slow overcurrent protection seemed acceptable. Could up the resistor value and go with a smaller Mylar cap if necessary.

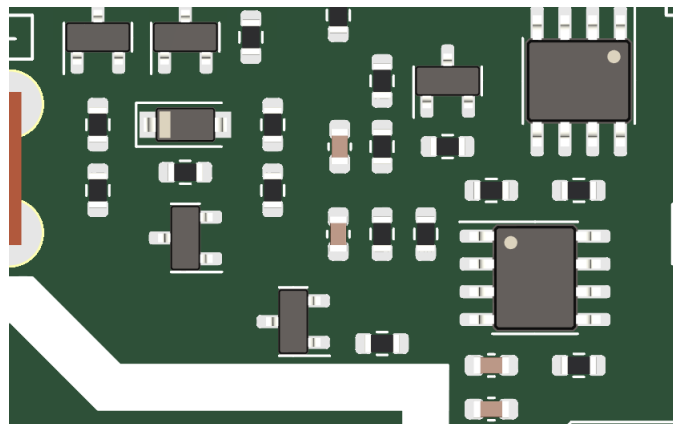# Voltage Sensing and Undervoltage Detection

Schematic
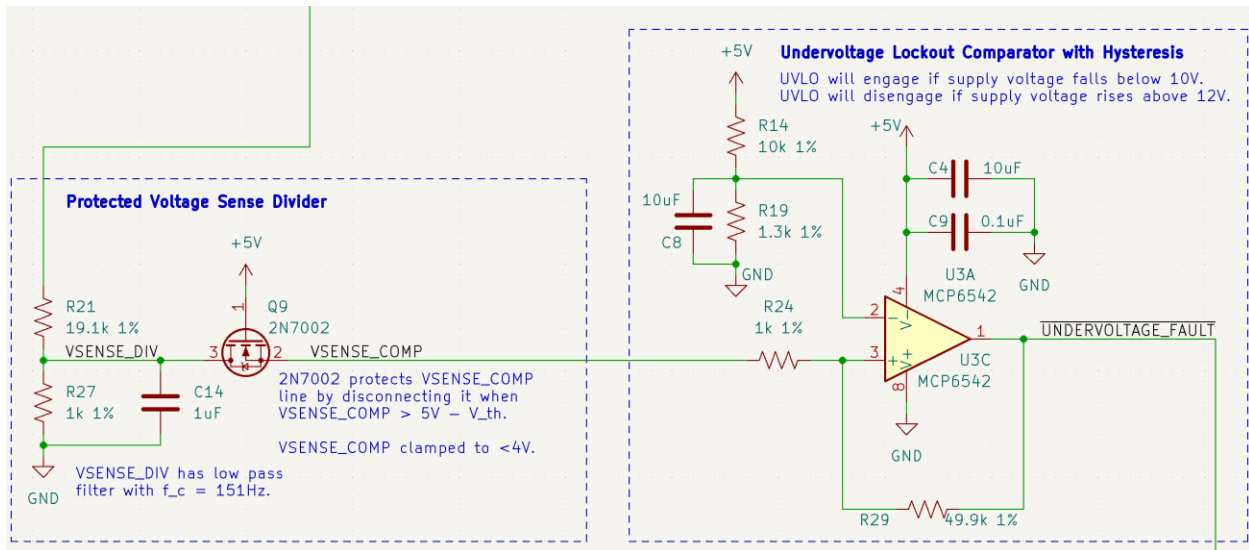
Voltage detection is accomplished with a simple voltage divider that includes a filter capacitor. Protection from overvoltage events is provided with a 2N7002 signal NMOS transistor (Q9) that is connected drain-first. If the divided voltage goes above 5V-Vth (where Vth is the threshold voltage of the MOSFET), the NMOS transistor turns off and isolates any downstream devices from the divided voltage signal.

Undervoltage protection is provided with a comparator that triggers an undervoltage fault on the shared FAULT_TIMER bus whenever the voltage drops below the level where the primary load PMOS switch can be fully turned on (around 10V). Hysteresis is provided to avoid undervoltage lockout oscillation while the supply voltage increases above the lockout threshold.

Calculations

| Voltage Sense Parameters			
Sense Divider			
R_vsense,top	19	kOhms	Voltage sense divider top resistor.
R_vsense,bot	1	kOhms	Voltage sense divider bottom resistor.
C_vsense	1	uF	Voltage sense divider bottom filter capacitor.
f_vsense,c	0.151	kHz	Voltage sense divider corner frequency.
A_vsense	0.05	V/V	Voltage sense divider gain.
V_vsense,protection,th	2.10	V	Thresold voltage of voltage sense divider protection MOSFET (typical). Used values from 2N7002 datasheet (https://www.onsemi.com/pdf/datasheet/nds7002a-d.pdf). NOTE: make sure the MCU can handle voltages when MOSFET has minimum threshold voltage, and that sense range is not terribly impaced when MOSFET has maximum threshold voltage!
Undervoltage Protection Comparator			
V_uvlo	11	V	Undervoltage lockout voltage. Set to satisfy acceptable minimum R_ds,on for PMOS switch in minimum supply voltage scenario, taking into account headroom required for PMOS drive circuit.
V_uvlo,div	0.55	V	Divided undervoltage lockout threshold.
V_uvlo,hysteresis	1	V	Hysteresis voltage (one side) of supply voltage for undervoltage lockout.
V_uvlo,top	5	V	Logic supply voltage for UVLO comparator circuit.
V_uvlo,div,tlh	0.6	V	Voltage sense divided voltage UVLO low to high transition voltage.
V_uvlo,div,thl	0.5	V	Voltage sense divided voltage UVLO high to low transition voltage.
R_uvlo,in	1	kOhms	
V_uvlo,oh	5	V	
R_uvlo,f	50	kOhms	
V_uvlo,ref	0.59	V	
V_TLH_CHECK	0.60	V	
V_THL_CHECK	0.5	V	
R_uvlo,ref,top	10	kOhms	
R_uvlo,ref,bot	1.3	kOhms	

PCB Layout

Shared Fault Bus with Sustained Latch

Schematic

Undercurrent and overcurrent fault events can be too brief for a microcontroller to read without using interrupts, and if an undervoltage or overcurrent fault occurs but is immediately cleared, the load can enter a cycle of continuous faulting where the load is disabled, the fault is cleared, the load is re-enabled, and the fault occurs again. This can result in an unwanted PWM-like behavior where the load current or voltage is regulated to a level near the trip threshold, possibly resulting in damage to components or wiring and suppressing reporting of the system fault. The solution to this problem is to latch any fault that occurs for a minimum amount of time, such that the microcontroller can easily report it, and the automatic "retry" time where the load switch is re-enabled after the fault is cleared is long enough that intermittent repeating faults do not result in any long term damage.
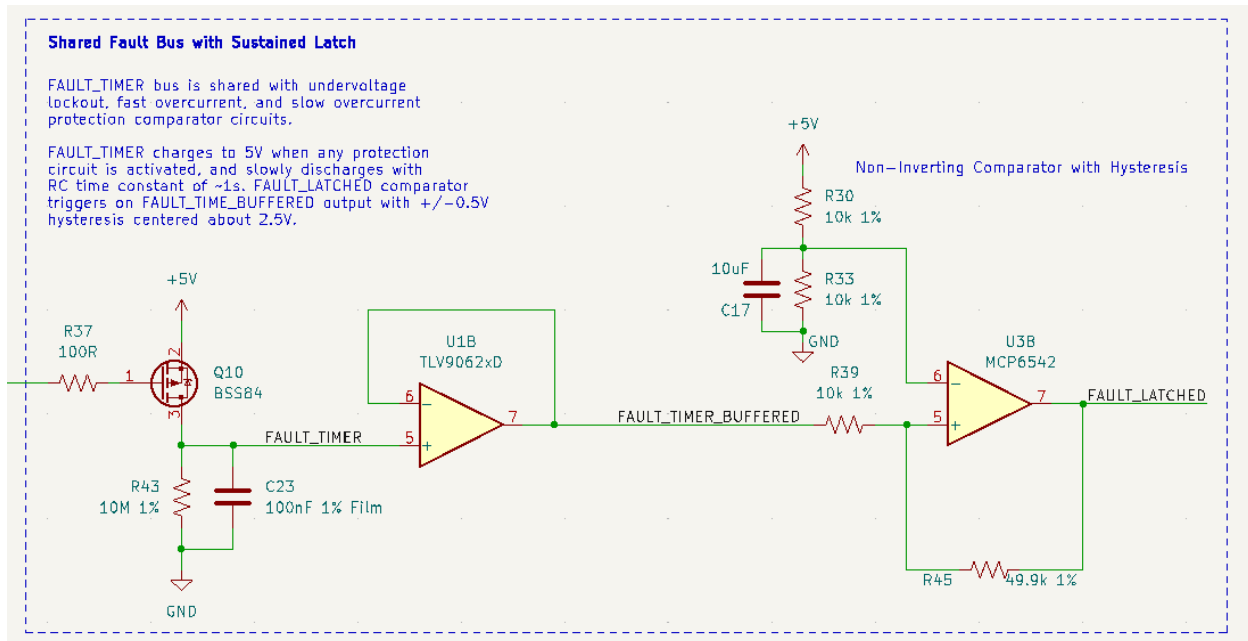

The various fault lines (SLOW_OVERCURRENT_FAULT, FAST_OVERCURRENT_FAULT, and UNDERVOLTAGE_FAULT) are each connected to a PMOS signal MOSFET that charges an RC timing circuit when any fault is tripped. The image above shows the fault MOSFET for the undervoltage protection circuit (Q10). The attached FAULT_TIMER RC timing circuit (R43 and C23) is charged up to +5V whenever any fault is tripped, and the timing capacitor (C23) slowly discharges through the parallel resistor (R43). The resulting RC time constant of around 1 second is used to keep the FAULT_LATCHED net HI until the FAULT_TIMER net has discharged below the threshold set by the fault timer comparator, which reads the FAULT_TIMER net through an op-amp buffer in order to not disturb its discharge time.

Calculations

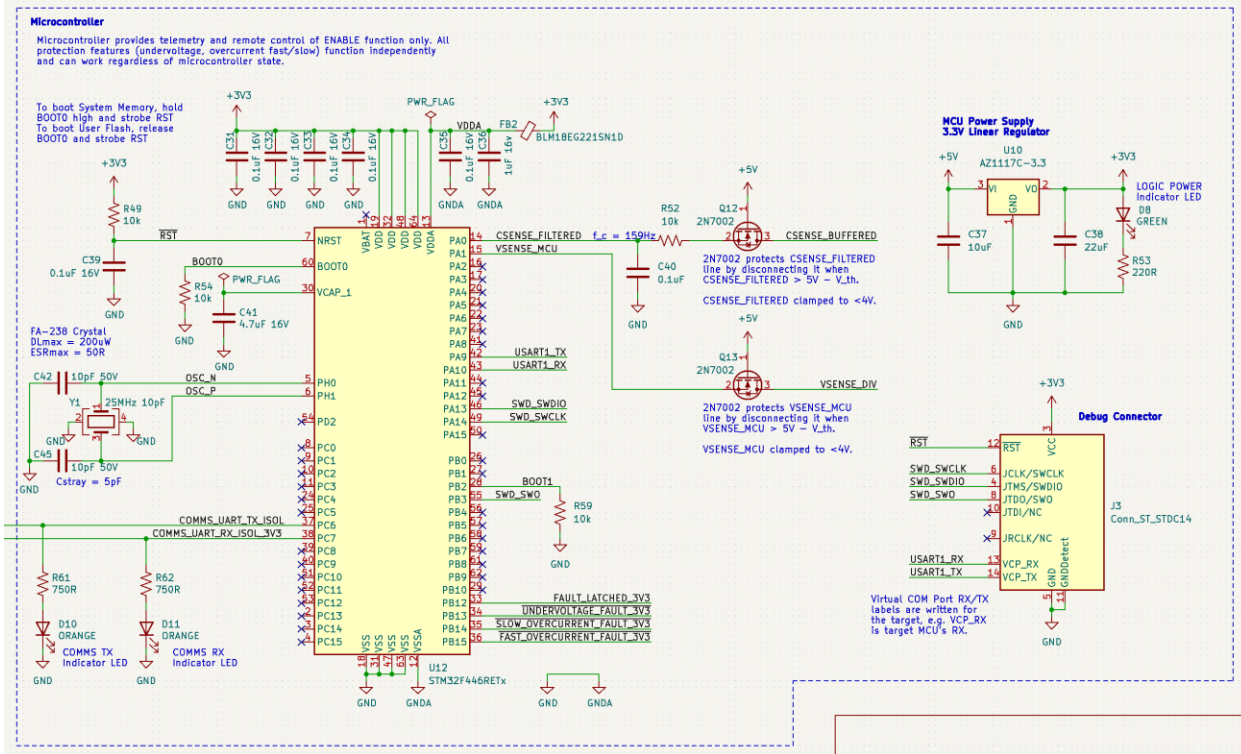| Fault Latch			
T_fault,latch	1	s	Desired RC latch time constant.
R_fault,latch	10	Mohms	Fault latch circuit timing cap discharge resistor.
C_fault,latch	100	nF	Fault latch circuit timing cap.

PCB Layout

A Mylar timing cap is used for the FAULT_TIMER RC circuit due to its well-controlled capacitance.
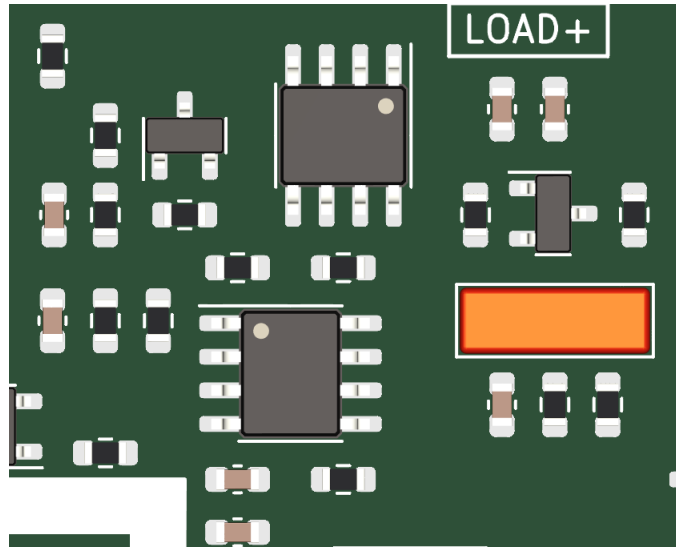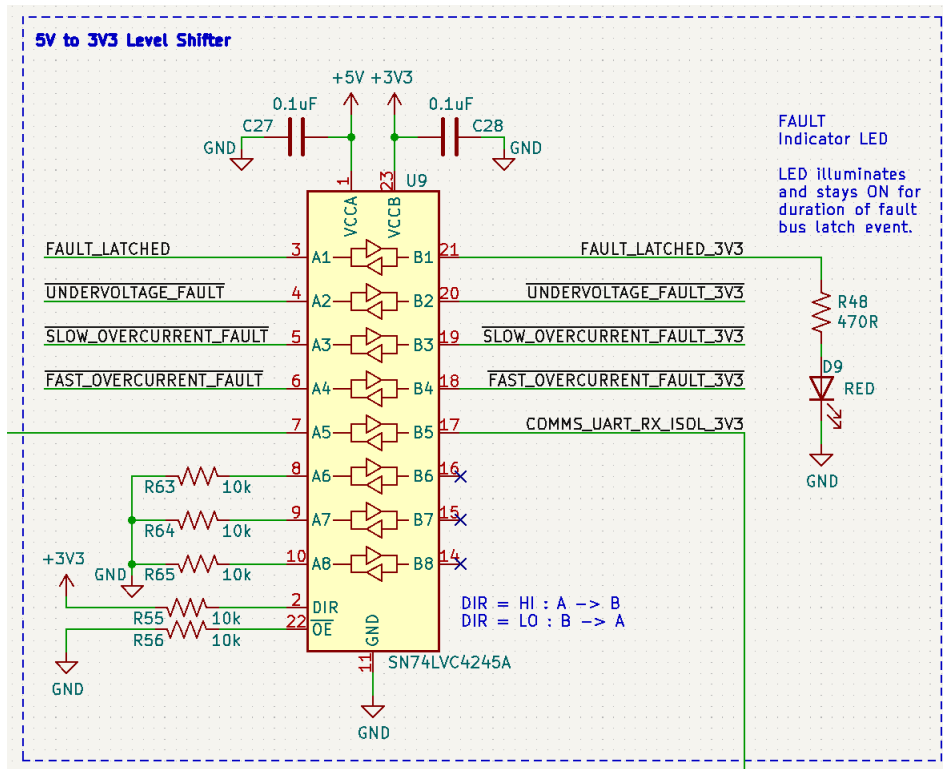
Microcontroller

Schematic

An STM32F446RET6 was selected as the microcontroller due to its ubiquitous interfaces, reasonable supply chain availability, well documented environmental ratings, and previous familiarity. The STM32's internal 12-bit ADC is used for voltage and current sensing, while digital inputs are used to read bus fault signals. An external 25MHz crystal is provided in order to provide a more accurate clock frequency, which is helpful for UART at higher baud rates. USART peripherals are used in asynchronous mode as both a debug UART interface (USART1) and a primary device communication interface (USART6, on PC6 and PC7). Programming of the device is achieved over Serial Wire Debug (SWD) via a standard STDC14 debug connector.

The microcontroller is provided with a separate 5V to 3.3V linear regulator power supply, since it is the only device on the board that requires 3.3V for operation. Analog pins are provided with separate bypass capacitors, and the analog power supply is linked to the main 3.3V power supply with a ferrite bead for noise suppression. Additional protection and filtering is provided on the current and voltage sense lines in order to reduce noise and clamp voltages to a safe range for the microcontroller. An additional RC filter is not needed on the voltage sense line since the corner frequency is already in a desirable range due to the RC filter built into the primary voltage divider (not shown).

5V to 3V3 Level Shifter

SN74LVC4245A (U9)

FAULT_LATCHED → A1 (3) / B1 (21) → FAULT_LATCHED_3V3
UNDERVOLTAGE_FAULT → A2 (4) / B2 (20) → UNDERVOLTAGE_FAULT_3V3
SLOW_OVERCURRENT_FAULT → A3 (5) / B3 (19) → SLOW_OVERCURRENT_FAULT_3V3
FAST_OVERCURRENT_FAULT → A4 (6) / B4 (18) → FAST_OVERCURRENT_FAULT_3V3
A5 (7) / B5 (17) → COMMS_UART_RX_ISOL_3V3
A6 (8) / B6 (16)
A7 (9) / B7 (15)
A8 (10) / B8 (14)

C27 0.1uF, C28 0.1uF, +5V, +3V3, GND

R63 10k, R64 10k, R65 10k, R55 10k, R56 10k

DIR (2), OE (22)

DIR = HI : A -> B
DIR = LO : B -> A

FAULT Indicator LED

LED illuminates and stays ON for duration of fault bus latch event.

R48 470R
D9 RED

A level shifter is needed to convert many of the 5V signals from elsewhere on the board to 3.3V logic levels. Unused inputs are pulled to GND to avoid oscillations on the level shifter outputs that would occur if the inputs were left floating.
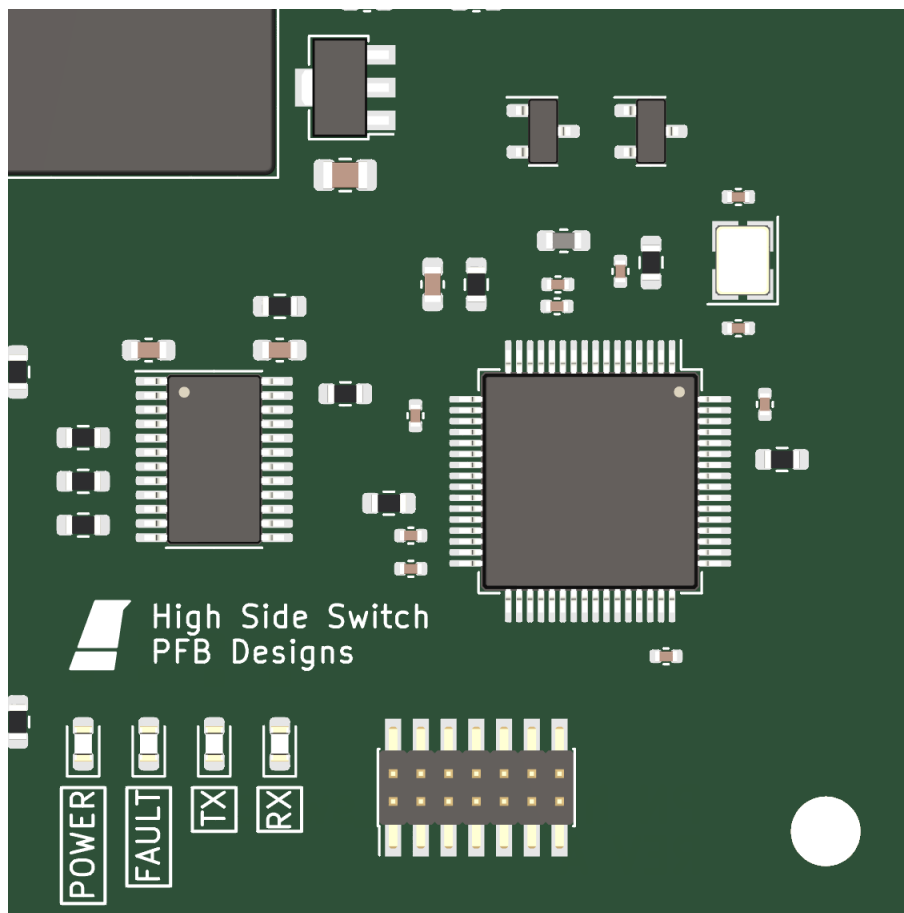
Indicator LEDs provide feedback to the user when the 3.3V power supply is on (green light), when a fault has been detected (red light), and when the primary device serial interface is transmitting or receiving (orange lights).

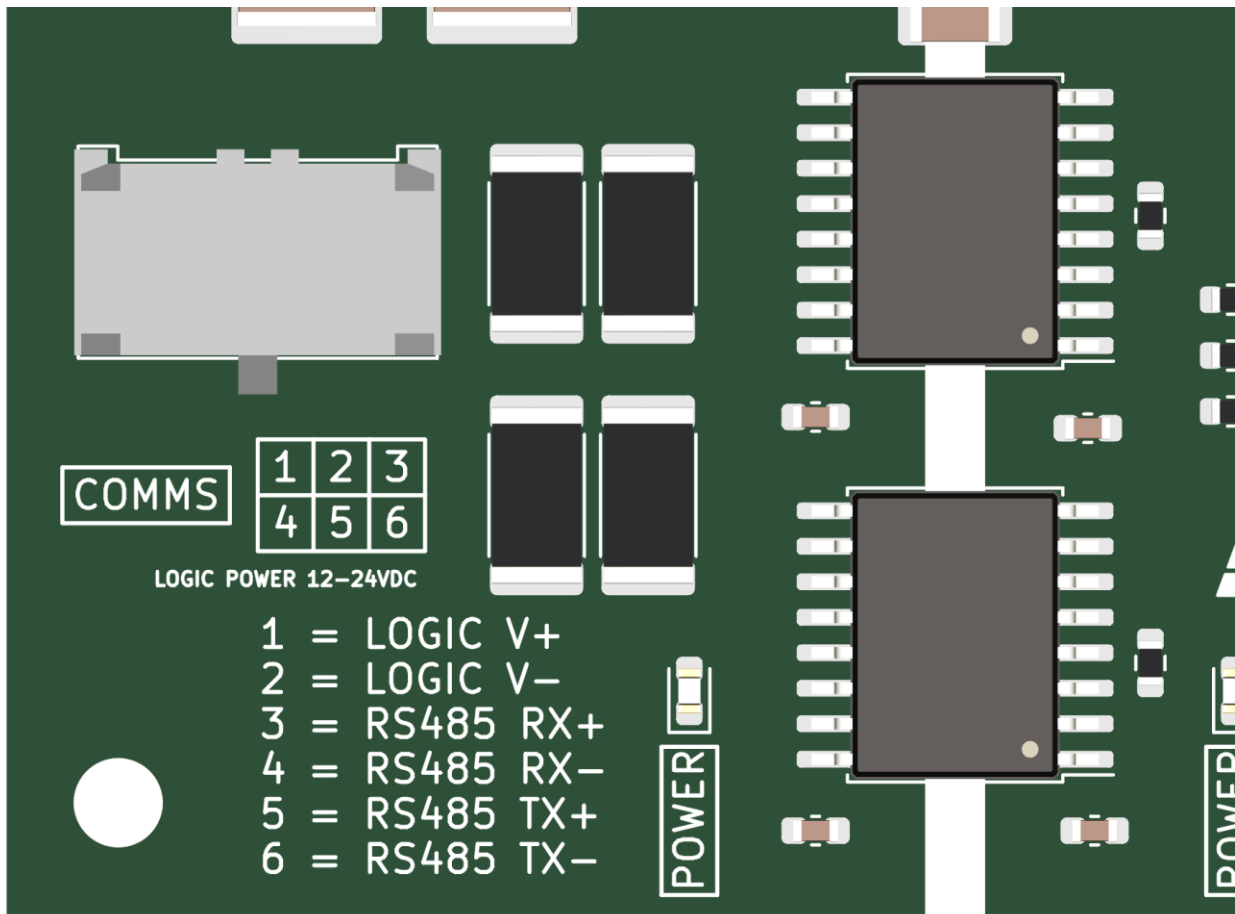# Isolated Full-Duplex RS-485 Communication Interface
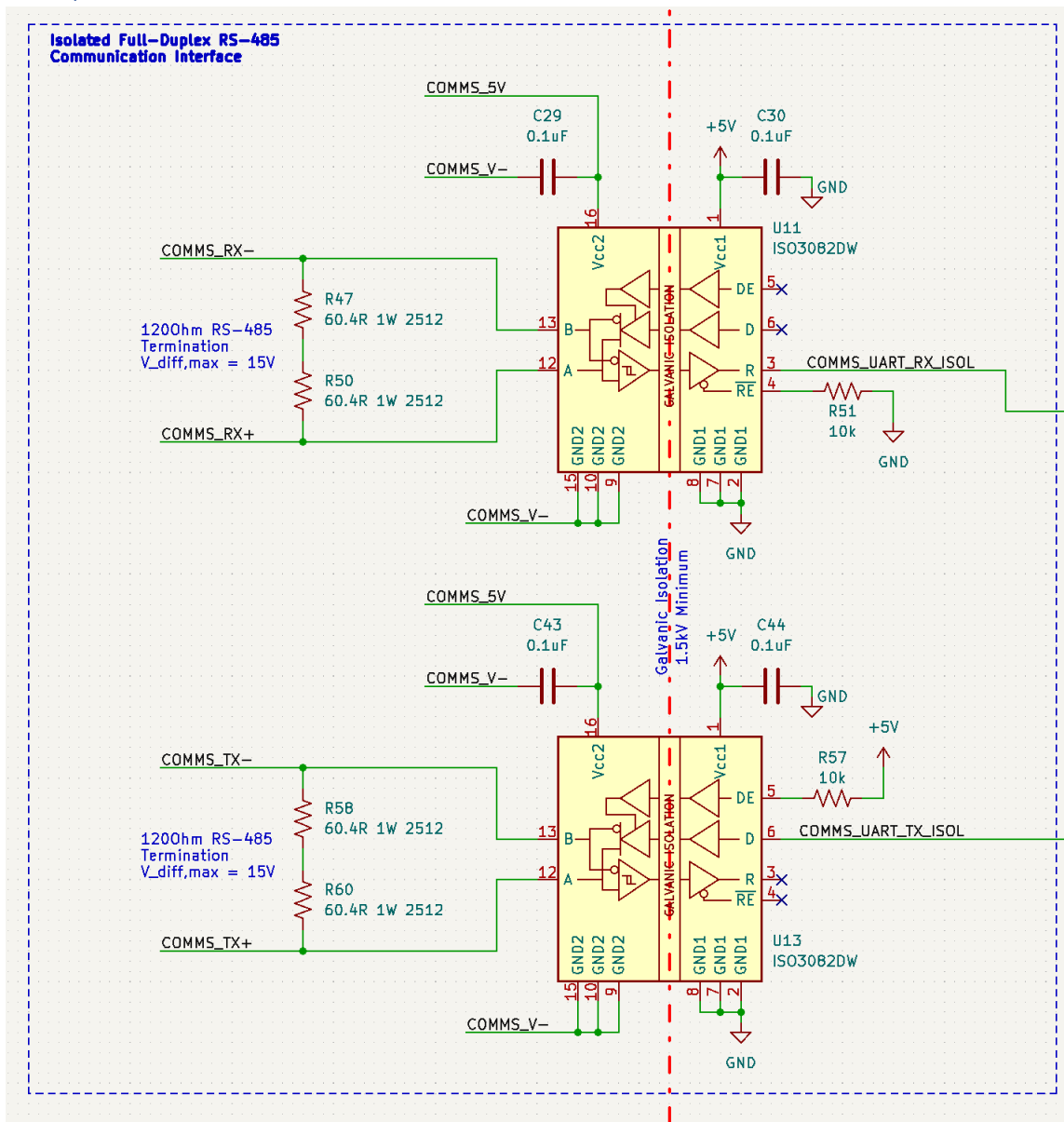
Device communication is conducted with UART over a galvanically isolated full-duplex RS-485 interface. Differentially-signaled RS-485 is immune to common mode interference and can run for thousands of feet under the right conditions, making it a good simple choice for long distance communication with the remote control computer. Since RS-485 is a fully digital interface, it can easily be isolated as shown in order to break any ground loops that might otherwise form in wiring harnesses, as well as provide protective separation between the communications bus and the primary DC power bus in the case of potentially hazardous voltage transients on one bus or the other.

Both TX and RX transceivers are terminated with a characteristic impedance of 120Ohms. The communication wiring harness should use a differential impedance of 120Ohms across the +/- signal wires for optimum performance. To reduce power dissipation, termination resistors (e.g. R58, R60) can be removed, in exchange for increased reflections and reduced performance. This tradeoff may be acceptable at low baud rates.

The isolated UART RX line is fed to the microcontroller's UART port via a 5V to 3.3V level shifter. The isolated UART TX line is driven directly by the microcontroller, since its voltage levels are compatible with a 3.3V TTL logic input.

EACH RS-485 transceiver is galvanically isolated internally and provided with separate power supplies on either side of the isolation barrier.

PCB Layout

COMMS

```
1  2  3
4  5  6
```

LOGIC POWER 12-24VDC

```
1 = LOGIC V+
2 = LOGIC V-
3 = RS485 RX+
4 = RS485 RX-
5 = RS485 TX+
6 = RS485 TX-
```

POWER

POWER

1.5kV Isolation barrier is denoted in white. Conformal coating is required to satisfy electrical spacing at full isolation voltage.

Logic and Communications Power Supplies
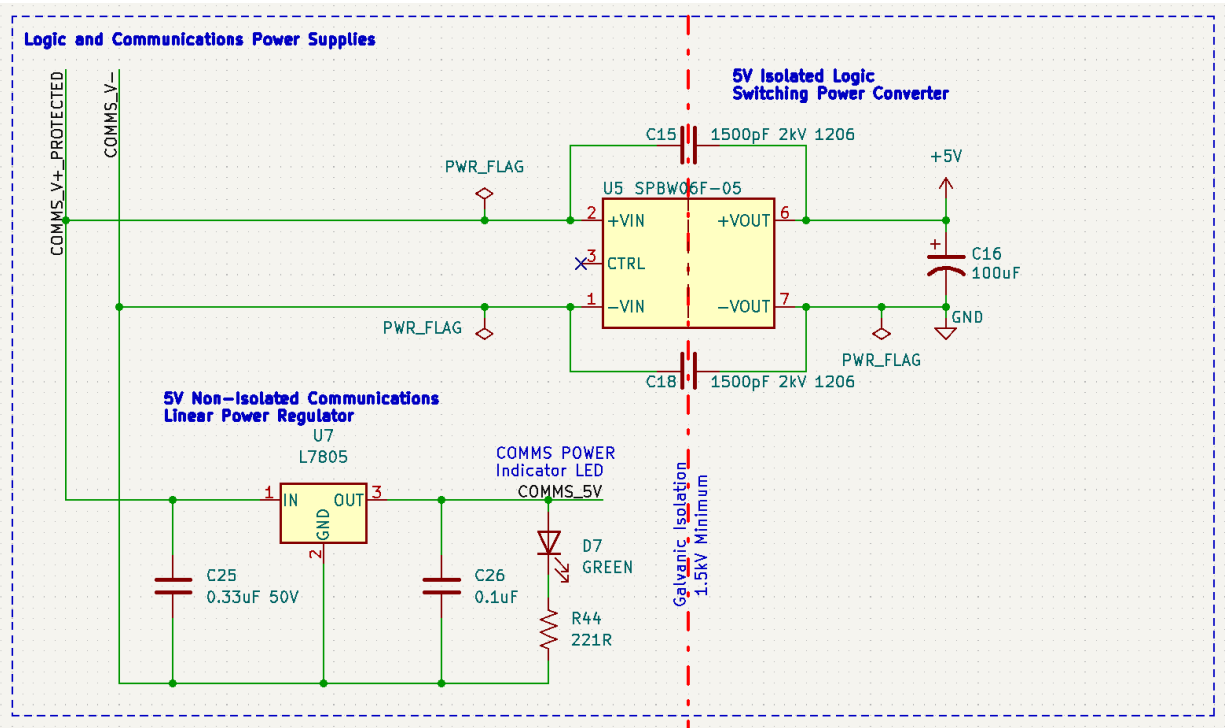
Power is supplied to the onboard communications and logic circuits via the COMMS connector. Non-isolated power is provided to the non-isolated side of the RS-485 transceivers via a linear regulator (U7), while isolated power is provided to the rest of the circuit through an isolated switching DC-DC converter (U5). The switching converter has an input voltage range of 9-36V while the linear regulator has an input range of up to 35V. The circuit is designed to accept a COMMS connector with 12-24VDC available across the LOGIC V+ and LOGIC V- pins.
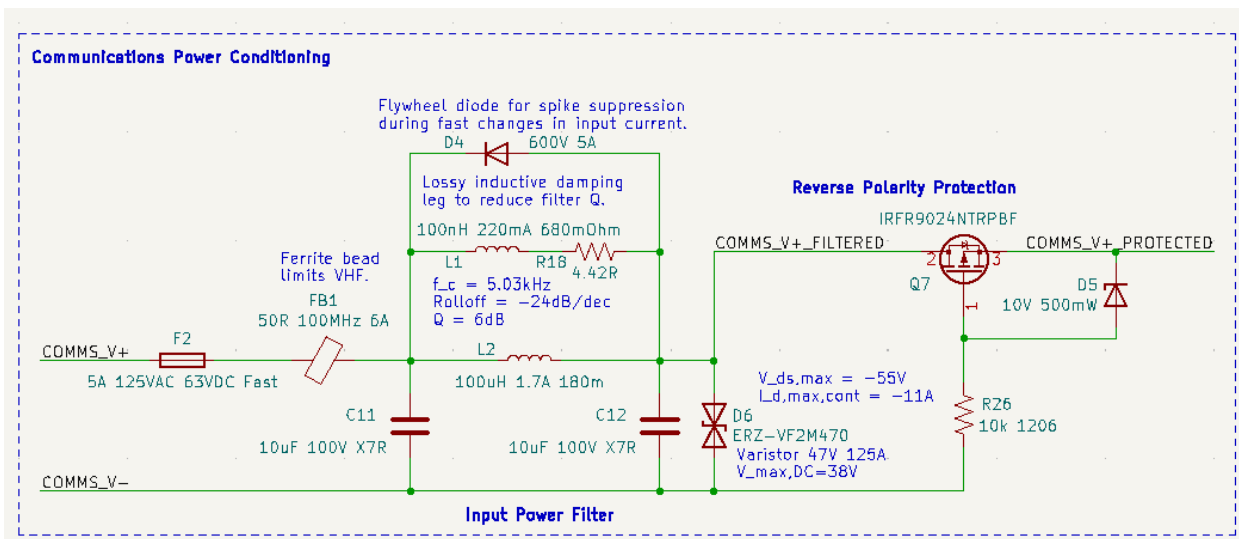
Protection is provided for the communications and logic circuit power supplies with a damped PI filter, input fuse, varistor, and reverse polarity protection circuit. The input PI filter and ferrite bead cut down on noise entering and leaving the device via the COMMS_V+ and COMMS_V- connections. Damping the inductor with a lossy parallel inductor allows significant reduction of device Q with small external components. A flywheel diode in parallel with the filter inductor suppresses voltage spikes resulting from sudden changes in input current. The reverse polarity protection circuit (Q7 and friends) is identical to the system power input reverse polarity protection circuit (Q1 and friends), but

uses smaller components since it only needs to sustain load currents up to around 1A. The varistor (D6) provides an additional level of protection by absorbing overvoltage pulses that pass through the PI filter and blowing the input fuse if necessary to disable the device during a large overvoltage event.

PCB Layout